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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/359,056	07/21/1999	BARMAK MANSOORIAN	08305/038001	2286

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/359,056	MANSOORIAN, BARMAK	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6 and 8-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,4,6 and 9-17* is/are allowed.

6)☒ Claim(s) *8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/24/2005, with respect to claims 1, 3, 4, 6, 9-13, 15 & 16 have been fully considered and are persuasive. The rejection of these claims has been withdrawn.

2. Applicant's arguments filed 10/24/2005 with respect to claim 8 have been fully considered but they are not persuasive.

Regarding claim 8, the Applicant asserts that Pain, Long and Pickering do not teach or disclose "an active impedance matching device, said active impedance matching device being adapted to match said output impedance of said image processing portion to said input impedance of said image receiving portion."

In response, the Examiner respectfully disagrees with the Applicant. Long teaches a current mode driver for integrated circuits (chips) comprising an active impedance matching device that is implemented in CMOS and being adapted to match an output impedance of transmitter of a chip (40) to an input impedance of receiver of another chip (42). See Long, Figs. 3 & 4, col. 4, lines 10-63. The implementation of CMOS current mode driver and an active impedance matching device in Long reduces power dissipation in digital circuits by transmitting current mode signal with relatively small current swings (see Long, col. 2, lines 38-40 and col. 4, lines 10-15). Long also teaches that the current mode driver has an output voltage swing of less than 0.5 volts. See Table II in col. 7 for CMOS current mode, wherein current swing of 1mA must generate a relatively low voltage swing of less than 0.5 volts at the output of transmitter 40

over transmission line 44 since it is required a current swing between 10 mA to 40 mA to generate a voltage swing of at least 0.5 volts (see Long, col. 1, lines 25-55). Thus, the limitations required in claim 8 are met by the combined teachings of Pain, Long and Pickering as analyzed in the previous Office Action.

Drawings

3. The drawings received on 10/24/2005 are accepted. These drawings are Figs. 1 - 9b.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (US 5,886,659) in view of Long et al (US 5,811,984) and in further view of Pickering et al (US 5,050,194).

Regarding claim 8, Pain discloses an image sensor comprising:

an image acquisition portion (100, 112 shown in Figs. 1A-1C, col. 3, lines 52-63);

an image processing portion (ADC array 118), receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS outputs having an output impedance; said image processing portion producing a current

mode output or so called a current mode driver (see Fig. 1C; col. 1, line 55 – col. 2, line 7; col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16). It is noted that the output impedance is inherent at the ADC array output. Since the ADC array is configured with CMOS current driving mode, the impedance must exist at the ADC array output and throughout transmission line(s).

Pain also *implicitly* discloses another separate portion (i.e., another chip) to be connected to an output of ADC array for receiving digital image data output from the ADC array (see Figs. 1A-1C). Thus, "an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs, and said image receiving portion receiving current mode output" are suggested by Pain in order to form a complete imaging system having CMOS compatible components (see col. 2, lines 5-7 for a consistent CMOS compatible imaging system).

Therefore, it would have been obvious to one of ordinary skill in the art to recognize another chip connected to the digital output from the image processing portion (ADC array 118) as an image receiving portion which would be also configured in CMOS having input characteristics compatible with the digital output of the image processing portion to form a complete imaging system for capturing and processing image signals.

Pain does not explicitly disclose the CMOS outputs being differential outputs and an active impedance matching device being adapted to match said output impedance of said image processing portion to said input impedance of said image receiving portion, and a current mode driver having an output voltage swing of less than 0.5 volts.

Long teaches a current mode driver for integrated circuits (IC chips) comprising an active impedance matching device that is implemented in CMOS and being adapted to match an output

impedance of transmitter of a chip (40) to an input impedance of receiver of another chip (42). See Long, Figs. 3 & 4, col. 4, lines 10-63. Long also teaches that the current mode driver has an output voltage swing of less than 0.5 volts. See Table II in col. 7 for CMOS current mode in which current swing of 1mA must generate a relatively low voltage swing of less than 0.5 volts at the output of transmitter 40 over transmission line 44 since it is required a current swing between 10 mA to 40 mA to generate a voltage swing of at least 0.5 volts (see Long, col. 1, lines 25-55). The implementation of CMOS current mode driver and an active impedance matching device taught by Long reduces power dissipation in digital circuits by transmitting current mode signal with relatively small current and voltage swing (see Long, col. 2, lines 38-40 and col. 4, lines 10-15).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Pain and Long to construct an image sensor having an image receiving portion and an active impedance matching device for actively matching an output impedance of an image processing portion to an input impedance of an image receiving portion while maintaining an output voltage swing of less than 0.5 volts for the current mode driver so that power dissipation would be reduced.

Pain and Long are silent about CMOS differential outputs of the image processing portion. Pickering teaches a CMOS differential output implemented as a CMOS differential output driver (see Pickering, Fig. 1) for driving current mode signals over a transmission line (5) between chips (Pickering, col. 2, lines 45-50). The CMOS differential output provides advantage of minimizing the effects of common-mode noise beside the advantage of matching impedance (Pickering, col. 2, lines 16-20).

Therefore, it would have been obvious to one of ordinary skill in the art to further modify the combined apparatus in Pain and Long to incorporate a differential output/input driver using CMOS technology for transmitting and receiving off-chip image data as taught by Pickering so as to reduce common-mode noise.

Allowable Subject Matter

5. Claims 1, 3, 4, 6, 9-17 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding independent claim 1, the prior art of record fails to teach or fairly suggest the combination of all limitations required in claim 1 that includes *"...an active impedance matching device having a current source, said active impedance matching device being adapted to match said output impedance of said image processing portion to said input impedance of said image receiving portion by adjusting, with said current source, a bias current through said at least a pair of transistors."*

Regarding independent claim 11, the prior art of record also fails to teach or fairly suggest the combination of all limitations required in claim 11 that includes *"...an impedance matching device, said impedance matching device being adapted to match an output impedance of said image acquisition portion to an input impedance of said image processing portion by adjusting bias current through at least one biased device in a way that renders said input impedance relatively independent of an input current..."*

Regarding independent claim 15, the prior art of record also fails to teach or fairly suggest the combination of all limitations required in claim 15 that includes *"...an impedance*

matching device having a current source, said impedance matching device being adapted to match an output impedance of said image acquisition portion to an input impedance of said image processing portion by adjusting bias current, from said current source, through said at least a pair of transistors in a way that renders said input impedance relatively independent of an input current."

Regarding independent claims 14 & 17, the prior art of record also fails to teach or fairly suggest the combination of all limitations required in each of claims 14 and 17 that includes "*...said image acquisition portion and said image processing portion operate at substantially zero voltage.*"

Regarding claims 3, 4, 6, 9, 10, 12 & 13, these claims directly or indirectly depend from claim 1.

Regarding claim 16, this claim depends from claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 7:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

TUAN HO
PRIMARY EXAMINER